AMENDMENTS

IN THE CLAIMS:

Please amend claims 1 and 22 as follows below.

1. (Currently amended) An integrated circuit, comprising:

an array of ferroelectric memory cells, each cell having a capacitor stack having an upper electrode, a lower electrode, and a single ferroelectric core layer with a crystallization in the (001) family, wherein at least 40% of the domains of the single ferroelectric core layer are functionally oriented with respect to the capacitor stack, wherein at least one of the capacitor stacks comprises a conductive contact formed thereunder and wherein the conductive contact has a cross section near a contact portion with the bottom portion of the capacitor stack that is about as large or larger than that of the ferroelectric cores.

2. (Original) The integrated circuit of claim 1, wherein from about 45 to about 75% of the domains are functionally oriented with respect to the capacitor stack.

3. (Original) The integrated circuit of claim 1, wherein the ferroelectric cores are PZT cores and the PZT of each core has a switched polarization of at least about 60 μC/cm2.

4. (Previously presented) The integrated circuit of claim 1, further comprising:

a dielectric layer covering the array of memory cells, the dielectric layer having a conductive contact over each ferroelectric core, the conductive contacts each having a cross section about as large or larger than that of the ferroelectric cores.

5. (Original) The integrated circuit of claim 1, wherein electrodes adjacent opposing sides of the ferroelectric cores have a collective thickness of at least about 200 nm thick.

6-20. (cancelled)

21. (Previously presented) The integrated circuit of claim 1, further comprising:

a dielectric layer covering the array of memory cells, the dielectric layer having an additional conductive contact over each ferroelectric core and upper electrode, the additional conductive contacts each having a cross section about as large or larger than that of the ferroelectric cores and extending through said dielectric layer to a metal interconnect layer.

22. (Currently amended) An integrated circuit, comprising:

an array of ferroelectric memory cells, each cell having a capacitor stack comprising:

a lower barrier layer;

a lower electrode over the barrier layer;

a single ferroelectric core layer with crystallization in the (001) family, wherein at least 40% of the domains of the single ferroelectric core layer are functionally oriented with respect to the capacitor stack;

an upper electrode over the single ferroelectric core layer; and

an upper barrier over the upper electrode;

wherein at least one of the capacitor stacks comprises a first conductive contact formed ~~there~~over the capacitor stack, and a second conductive contact formed ~~there~~under the capacitor stack, and wherein the first and second conductive contacts each have~~has~~ a cross section near a contact portion ~~with the top portion~~ of the capacitor stack ~~and the bottom portion of the stack~~ that is about as large or larger than that of the ferroelectric cores.